AiP74LVC/LVCH162373
16-bit D-type Transparent Latch; 10 Ω Series Termination Resistors; 5V Tolerance Inputs/Outputs; 3-state

Product Specification

Specification Revision History:

Version	Date	Description
2022-04-A0	2022-04	New
2023-11-A1	2023-11	Parameter modification

Contents

1、General Description

The AiP74LVC/LVCH162373 are 16-bit D-type transparent latches featuring separate D-type inputs with bus hold (AiP74LVCH162373 only) for each latch and 3-state outputs for bus-oriented applications.
The input can be driven from either 3.3V or 5V devices. This feature allows the use of this device in a mixed 3.3V and 5V environment.

Features:

- Supply voltage range:1.2V to 3.6V
- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- High-impedance when V_{CC}=0V
- Temperature range:-40℃ to +125℃
- Packaging information: TSSOP48

Ordering Information:

Tube packing specifications:

Type number	Packaging form	Markin+g code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74LVC162373 TA48.TB	TSSOP48	74LVC162373	38 PCS/tube	100 tube/box	3800 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm
AiP74LVCH162373 TA48.TB	TSSOP48	74LVCH162373	38 PCS/tube	100 tube/box	3800 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74LVC162373 TA48.TR	TSSOP48	74LVC162373	2000 PCS/reel	2000 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm
AiP74LVCH162373 TA48.TR	TSSOP48	74LVCH162373	2000 PCS/reel	2000 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm

Note 1: “XX” refers to variable content, meaning year and package batch serial number.
Note 2: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

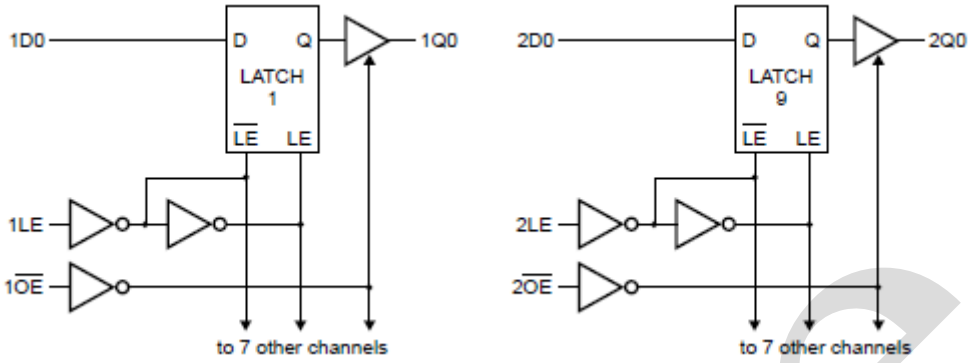
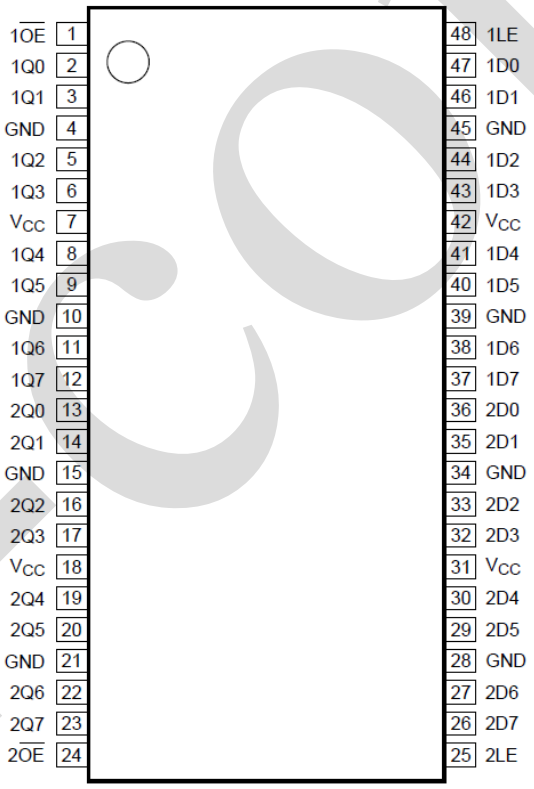


Figure 1. Logic diagram

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	$1\overline{OE}$	output enable input (active LOW)
24	$2\overline{OE}$	output enable input (active LOW)
48	1LE	latch enable input (active HIGH)
25	2LE	latch enable input (active HIGH)

4,10,15,21,28,34,39,45	GND	ground (0V)
7,18,31,42	V_{CC}	supply voltage
2,3,5,6,8,9,11,12	1Q0 to 1Q7	data output
13,14,16,17,19,20,22,23	2Q0 to 2Q7	data output
47,46,44,43,41,40,38,37	1D0 to 1D7	data input
36,35,33,32,30,29,27,26	2D0 to 2D7	data input

2.4、Function Table

Operating modes	Input			Internal latch	Output nQ0 to nQ7
	nOE	nLE	nDn		
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

Note:

H=HIGH voltage level

h=HIGH voltage level one set-up time prior to the HIGH to LOW LE transition

L=LOW voltage level

l=LOW voltage level one set-up time prior to the HIGH to LOW LE transition

Z=high-impedance OFF-state

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+6.5	V
input voltage	V_I	-	-0.5	+6.5	V
output voltage	V_O	Active mode	-0.5	V_{CC}+0.5	V
		Power-down mode; V_{CC}=0V	-0.5	+6.5	V
		output 3-state	-0.5	+6.5	V
supply current	I_{CC}	-	-	100	mA
ground current	I_{GND}	-	-100	-	mA
input clamping current	I_{IK}	V_I < 0V	-50	-	mA
output current	I_O	V_O=0V to V_{CC}	-	±50	mA
output clamping current	I_{OK}	V_O > V_{CC} or V_O < 0V	-	±50	mA
storage temperature	T_{stg}	-	-65	+150	℃
Soldering temperature	T_L	10s	260		℃

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	1.2	-	3.6	V
input voltage	V_I	-	0	-	5.5	V
output voltage	V_O	Active mode	0	-	V_{CC}	V
		Power-down mode; V_{CC}=0V	0	-	5.5	V
		output 3-state	0	-	5.5	V
ambient temperature	T_{amb}	-	-40	-	+125	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Vcc	Conditions	Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	1.2V	-	1.08	-	-	V
		1.65V to 1.95V	-	0.65× V_{CC}	-	-	V
		2.3V to 2.7V	-	1.7	-	-	V
		2.7V to 3.6V	-	2.0	-	-	V
LOW-level input voltage	V_{IL}	1.2V	-	-	-	0.12	V
		1.65V to 1.95V	-	-	-	0.35× V_{CC}	V
		2.3V to 2.7V	-	-	-	0.7	V
		2.7V to 3.6V	-	-	-	0.8	V
HIGH-level output voltage	V_{OH}	1.65V to 3.6V	I_O=-100uA	V_{CC}-0.2	-	-	V
		1.65V	I_O=-2mA	1.2	-	-	V
		2.3V	I_O=-4mA	1.7	-	-	V
		2.7V	I_O=-6mA	2.2	-	-	V
		3.0V	I_O=-12mA	2.2	-	-	V
LOW-level output voltage	V_{OL}	1.65V to 3.6V	I_O=100uA	-	-	0.2	V
		1.65V	I_O=2mA	-	-	0.45	V
		2.3V	I_O=4mA	-	-	0.6	V
		2.7V	I_O=6mA	-	-	0.4	V
		3.0V	I_O=12mA	-	-	0.55	V
input leakage current	I_I	3.6V	V_I=5.5V or GND	-	-	±5	uA
OFF-state output current	I_{OZ}	3.6V	V_O=5.5V or GND	-	-	±5	uA
power-off leakage current	I_{OFF}	0V	V_I or V_O=5.5V	-	-	±10	uA
supply current	I_{CC}	3.6V	V_I=V_{CC} or GND; I_O=0A	-	-	20	uA
additional supply current	ΔI_{CC}	2.7V to 3.6V	per input pin; V_I=V_{CC}-0.6V; I_O=0A	-	-	500	uA
bus hold LOW current	I_{BHL}	1.65V;	V_I=0.58V[3][4]	10	-	-	uA
		2.3V	V_I=0.7V	30	-	-	uA

		3.0V	V_I=0.8V	75	-	-	uA
bus hold HIGH current	I_{BHH}	1.65V	V_I=1.07V[3][4]	-10	-	-	uA
		2.3V	V_I=1.7V	-30	-	-	uA
		3.0V	V_I=2.0V	-75	-	-	uA
bus hold LOW overdrive current	I_{BHLO}	1.95V[3][5]	-	200	-	-	uA
		2.7V	-	300	-	-	uA
		3.6V		500	-	-	uA
bus hold HIGH overdrive current	I_{BHHO}	1.95V[3][5]	-	-200	-	-	uA
		2.7V	-	-300	-	-	uA
		3.6V	-	-500	-	-	uA

Note:

[1] All typical values are measured at V_{CC}=3.3V (unless stated otherwise) and T_{amb}=25°C.

[2] The bus hold circuit is switched off when V_I>V_{CC} allowing 5.5V on the input pin.

[3] Valid for data inputs (AiP74LVCH162373) only; control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data inputs holds the input below the specified V_I level.

[5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

3.3.2、DC Characteristics 2

(T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Vcc	Conditions	Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	1.2V	-	1.08	-	-	V
		1.65V to 1.95V	-	0.65× V_{CC}	-	-	V
		2.3V to 2.7V	-	1.7	-	-	V
		2.7V to 3.6V	-	2.0	-	-	V
LOW-level input voltage	V_{IL}	1.2V	-	-	-	0.12	V
		1.65V to 1.95V	-	-	-	0.35× V_{CC}	V
		2.3V to 2.7V	-	-	-	0.7	V
		2.7V to 3.6V	-	-	-	0.8	V
HIGH-level output voltage	V_{OH}	1.65V to 3.6V	I_O=-100uA	V_{CC}-0.3	-	-	V
		1.65V	I_O=-2mA	1.05	-	-	V
		2.3V	I_O=-4mA	1.55	-	-	V
		2.7V	I_O=-6mA	2.05	-	-	V
		3.0V	I_O=-12mA	2.0	-	-	V
LOW-level output voltage	V_{OL}	1.65V to 3.6V	I_O=100uA	-	-	0.3	V
		1.65V	I_O=2mA	-	-	0.65	V
		2.3V	I_O=4mA	-	-	0.8	V
		2.7V	I_O=6mA	-	-	0.6	V
		3.0V	I_O=12mA	-	-	0.8	V
input leakage current	I_I	3.6V	V_I=5.5V or GND	-	-	±20	uA
OFF-state output current	I_{OZ}	3.6V	V_O=5.5V or GND	-	-	±20	uA
power-off	I_{OFF}	0V	V_I or V_O=5.5V	-	-	±20	uA

leakage current							
supply current	I_{CC}	3.6V	$V_I=V_{CC}$ or GND; $I_O=0A$	-	-	80	uA
additional supply current	ΔI_{CC}	2.7V to 3.6V;	per input pin; $V_I=V_{CC}$-0.6V; $I_O=0A$	-	-	5000	uA
bus hold LOW current	I_{BHL}	1.65V;	$V_I=0.58V$[3][4]	10	-	-	uA
		2.3V	$V_I=0.7V$	25	-	-	uA
		3.0V	$V_I=0.8V$	60	-	-	uA
bus hold HIGH current	I_{BHH}	1.65V	$V_I=1.07V$[3][4]	-10	-	-	uA
		2.3V	$V_I=1.7V$	-25	-	-	uA
		3.0V	$V_I=2.0V$	-60	-	-	uA
bus hold LOW overdrive current	I_{BHLO}	1.95V[3][5]	-	200	-	-	uA
		2.7V	-	300	-	-	uA
		3.6V		500	-	-	uA
bus hold HIGH overdrive current	I_{BHHO}	1.95V[3][5]	-	-200	-	-	uA
		2.7V	-	-300	-	-	uA
		3.6V	-	-500	-	-	uA

Note:

[1] All typical values are measured at V_{CC}=3.3V (unless stated otherwise) and T_{amb}=25°C.

[2] The bus hold circuit is switched off when $V_I>V_{CC}$ allowing 5.5V on the input pin.

[3] Valid for data inputs (AiP74LVCH162373) only; control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data inputs holds the input below the specified V_I level.

[5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

3.3.3、AC Characteristics 1

(T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Vcc	Conditions	Min.	Typ.	Max.	Unit
nDn to nQn propagation delay	t_{PLH}, t_{PHL}	1.2V	see Figure 4	-	12	-	ns
		1.65V to 1.95V		-	6.6	15.0	ns
		2.3V to 2.7V		-	3.5	7.4	ns
		2.7V		-	3.5	6.7	ns
		3.0V to 3.6V		-	3.0	5.9	ns
nLE to nQn propagation delay		1.2V	see Figure 5	-	14	-	ns
		1.65V to 1.95V		-	7.6	16.0	ns
		2.3V to 2.7V		-	4.0	7.9	ns
		2.7V		-	3.7	7.0	ns
		3.0V to 3.6V		-	3.4	6.1	ns
$n\overline{OE}$ to nQn enable time	t_{PZH}, t_{PZL}	1.2V	see Figure 6	-	18	-	ns
		1.65V to 1.95V		-	7.1	15.6	ns
		2.3V to 2.7V		-	4.0	8.2	ns
		V_{CC}=2.7V		-	4.2	7.5	ns
		3.0V to 3.6V		-	3.2	6.1	ns
$n\overline{OE}$ to nQn disable time	t_{PLZ}, t_{PHZ}	1.2V	see Figure 6	-	11	-	ns
		1.65V to 1.95V		-	4.2	8.5	ns

		2.3V to 2.7V		-	2.3	4.6	ns
		2.7V		-	3.2	4.8	ns
		3.0V to 3.6V		-	2.9	4.6	ns
nLE HIGH pulse width	tw	1.65V to 1.95V	see Figure 5	5.0	-	-	ns
		2.3V to 2.7V		4.0	-	-	ns
		2.7V		3.0	-	-	ns
		3.0V to 3.6V		3.0	2.0	-	ns
nDn to nLE set_up time	tsu	1.65V to 1.95V	see Figure 7	3.0	-	-	ns
		2.3V to 2.7V		2.5	-	-	ns
		2.7V		2.0	-	-	ns
		3.0V to 3.6V		2.0	1.0	-	ns
nDn to nLE hold time	th	1.65V to 1.95V	see Figure 7	2.5	-	-	ns
		2.3V to 2.7V		2.0	-	-	ns
		2.7V		0.9	-	-	ns
		3.0V to 3.6V		0.9	-1.0	-	ns

Note:Typical values are measured at T_{amb}=25℃ and V_{CC}=1.8V, 2.5V, 2.7V, and 3.3V respectively.

3.3.4、AC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Vcc	Conditions	Min.	Typ.	Max.	Unit
nDn to nQn propagation delay	t_{PLH}, t_{PHL}	1.65V to 1.95V	see Figure 4	-	-	17.2	ns
		2.3V to 2.7V		-	-	8.5	ns
		2.7V		-	-	8.5	ns
		3.0V to 3.6V		-	-	7.5	ns
nLE to nQn propagation delay		1.65V to 1.95V	see Figure 5	-	-	18.5	ns
		2.3V to 2.7V		-	-	9.1	ns
		2.7V		-	-	9.0	ns
		3.0V to 3.6V		-	-	8.0	ns
$\overline{nOE}$ to nQn enable time	t_{PZH}, t_{PZL}	1.65V to 1.95V	see Figure 6	-	-	17.9	ns
		2.3V to 2.7V		-	-	9.4	ns
		V_{CC}=2.7V		-	-	9.5	ns
		3.0V to 3.6V		-	-	8.0	ns
$\overline{nOE}$ to nQn disable time	t_{PLZ}, t_{PHZ}	1.65V to 1.95V	see Figure 6	-	-	9.8	ns
		2.3V to 2.7V		-	-	5.3	ns
		2.7V		-	-	6.0	ns
		3.0V to 3.6V		-	-	6.0	ns
nLE HIGH pulse width	tw	1.65V to 1.95V	see Figure 5	5.0	-	-	ns
		2.3V to 2.7V		4.0	-	-	ns
		2.7V		3.0	-	-	ns
		3.0V to 3.6V		3.0	-	-	ns
nDn to nLE set_up time	tsu	1.65V to 1.95V	see Figure 7	3.0	-	-	ns
		2.3V to 2.7V		2.5	-	-	ns
		2.7V		2.0	-	-	ns
		3.0V to 3.6V		2.0	-	-	ns
nDn to nLE	th	1.65V to 1.95V	see Figure 7	2.5	-	-	ns

hold time		2.3V to 2.7V		2.0	-	-	ns
		2.7V		0.9	-	-	ns
		3.0V to 3.6V		0.9	-	-	ns

4、Testing Circuit

4.1、DC Testing Circuit

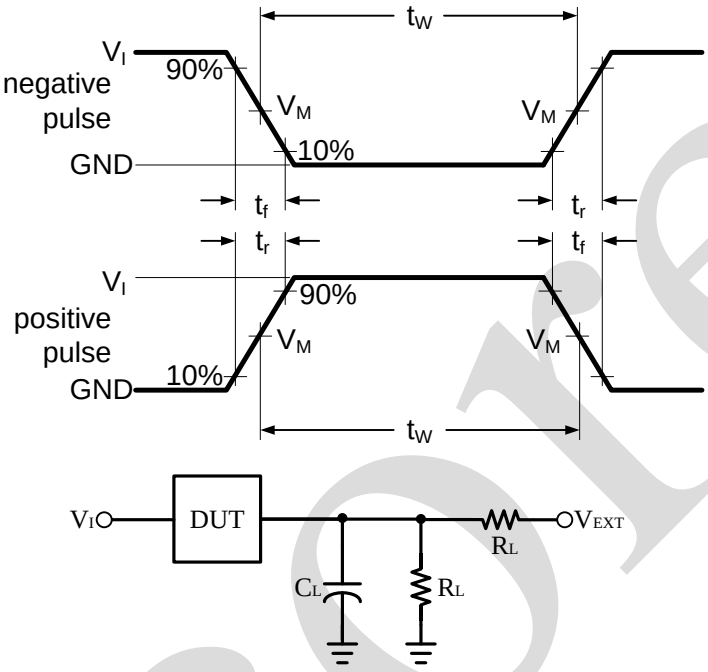


Figure 3. Load circuit

C_L includes probe and jig capacitance.

R_L=Load resistance.

4.2、AC Testing Circuit

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}/t_{PHL}	t_{PLZ}/t_{PZL}	t_{PHZ}/t_{PZH}
1.2V	V_{CC}	≤ 3ns	30pF	1kΩ	Open	2×V_{CC}	GND
1.65V to 1.95V	V_{CC}	≤ 3ns	30pF	1kΩ	Open	2×V_{CC}	GND
2.3V to 2.7V	V_{CC}	≤ 3ns	30pF	500Ω	Open	2×V_{CC}	GND
2.7V	V_{CC}	≤ 3ns	50pF	500Ω	Open	2×V_{CC}	GND
3.0V to 3.6V	V_{CC}	≤ 3ns	50pF	500Ω	Open	2×V_{CC}	GND

4.2、AC Testing Waveforms

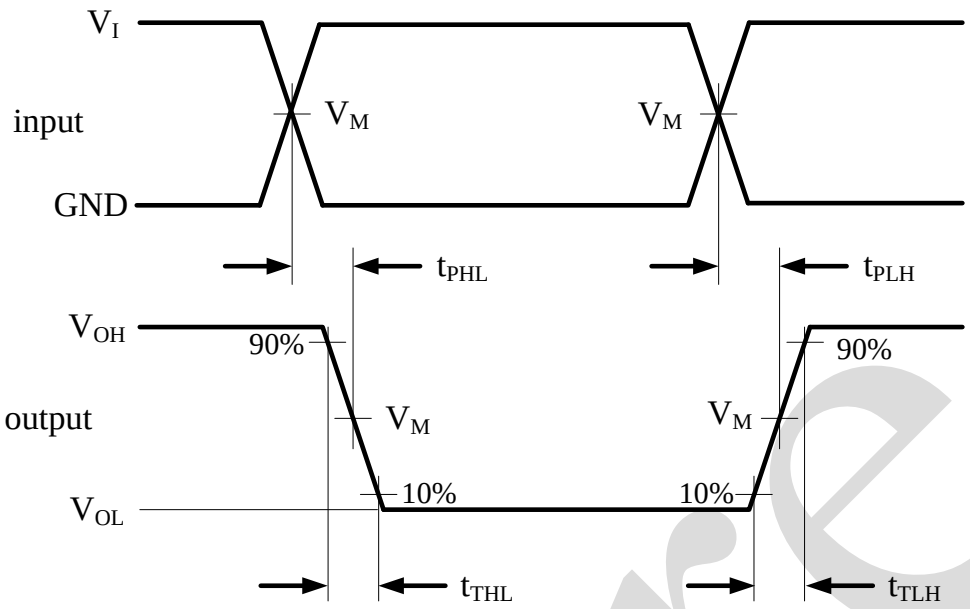


Figure 4. The data input (D) to output (Q) propagation delays

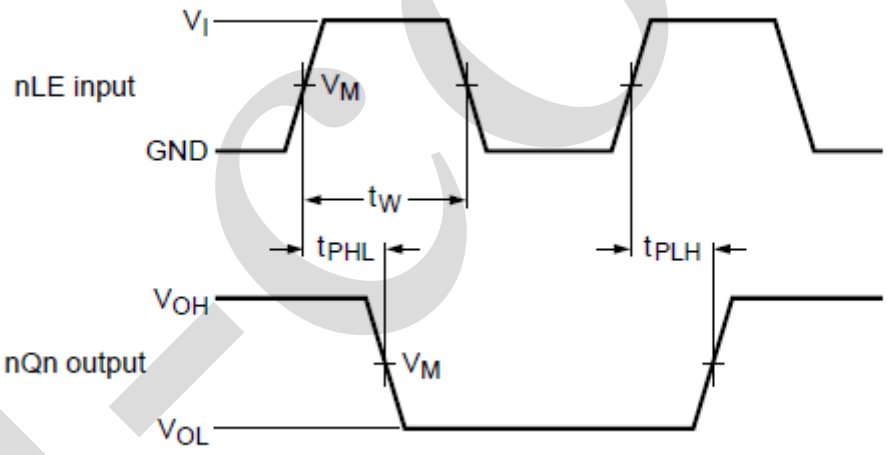


Figure 5. Latch enable (nLE) pulse width, and the latch enable input to output (nQn) propagation delays

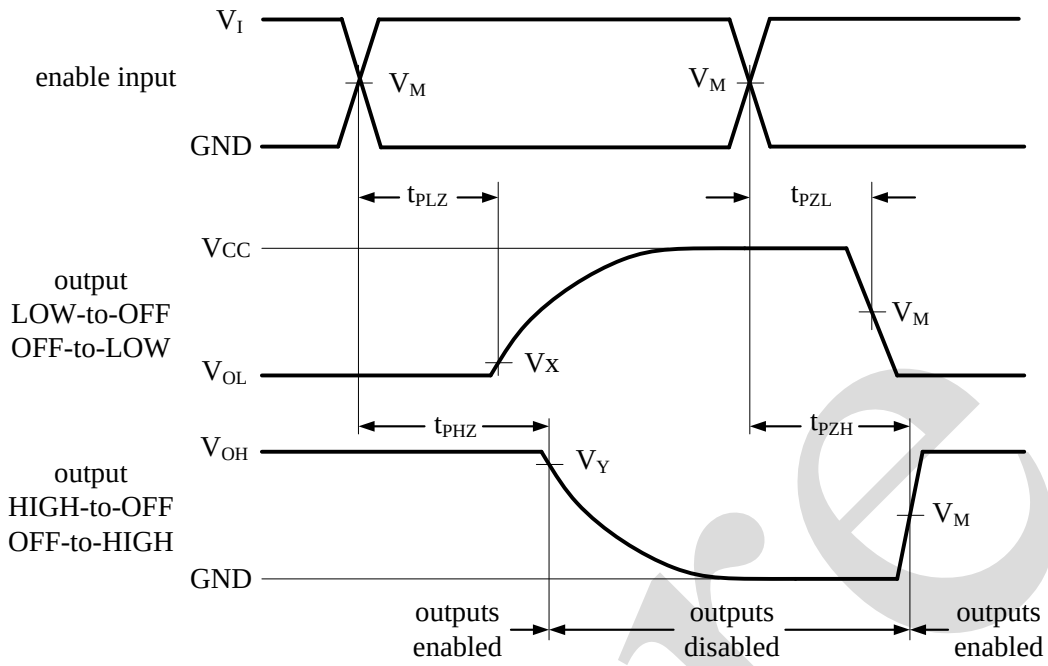


Figure 6. 3-state enable and disable times

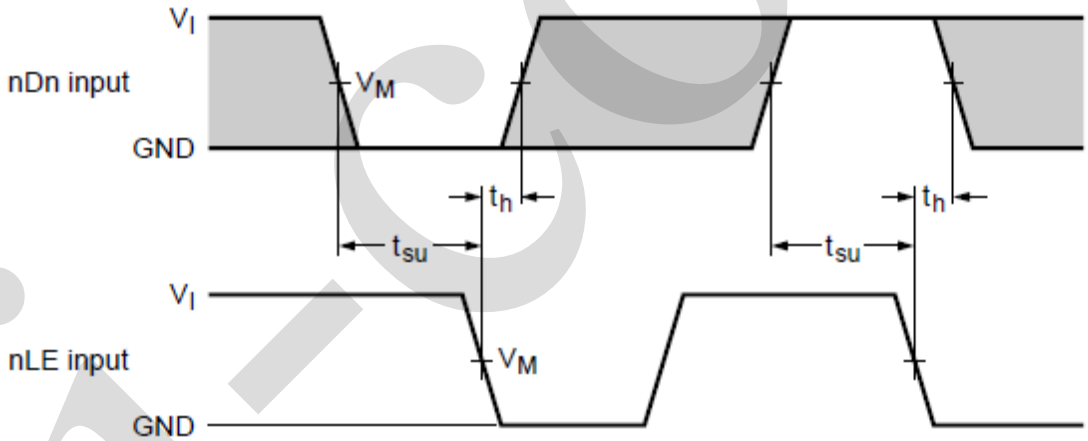


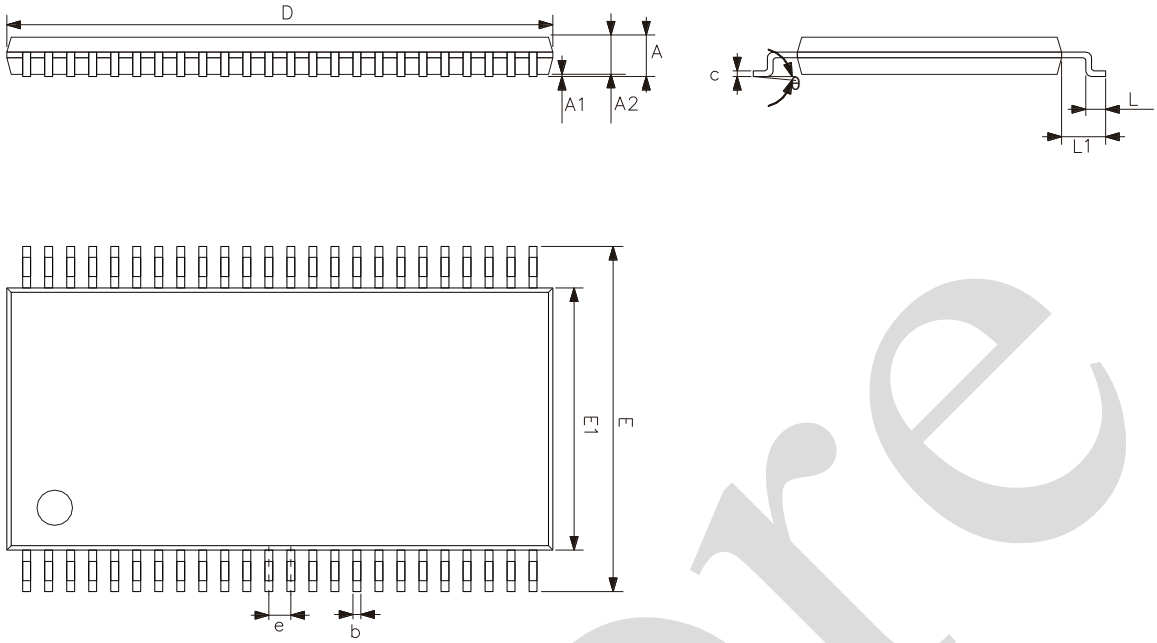
Figure 7. Data set-up and hold times for the nDn input to the nLE input

4.3、Measurement Points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.2V	0.5×V_{CC}	0.5×V_{CC}	V_{OL}+0.15V	V_{OH}-0.15V
1.65V to 1.95V	0.5×V_{CC}	0.5×V_{CC}	V_{OL}+0.15V	V_{OH}-0.15V
2.3V to 2.7V	0.5×V_{CC}	0.5×V_{CC}	V_{OL}+0.15V	V_{OH}-0.15V
2.7V	0.5×V_{CC}	0.5×V_{CC}	V_{OL}+0.3V	V_{OH}-0.3V
3.0V to 3.6V	0.5×V_{CC}	0.5×V_{CC}	V_{OL}+0.3V	V_{OH}-0.3V

5、Package Information

5.1、TSSOP48



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.03	0.15
A2	0.82	1.05
b	0.17	0.27
c	0.12	0.22
D	12.40	12.60
E	7.90	8.30
E1	6.00	6.20
e	0.50	
L	0.35	0.75
L1	1.00	
θ	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

We recommend you to read this chapter carefully before using this product.

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